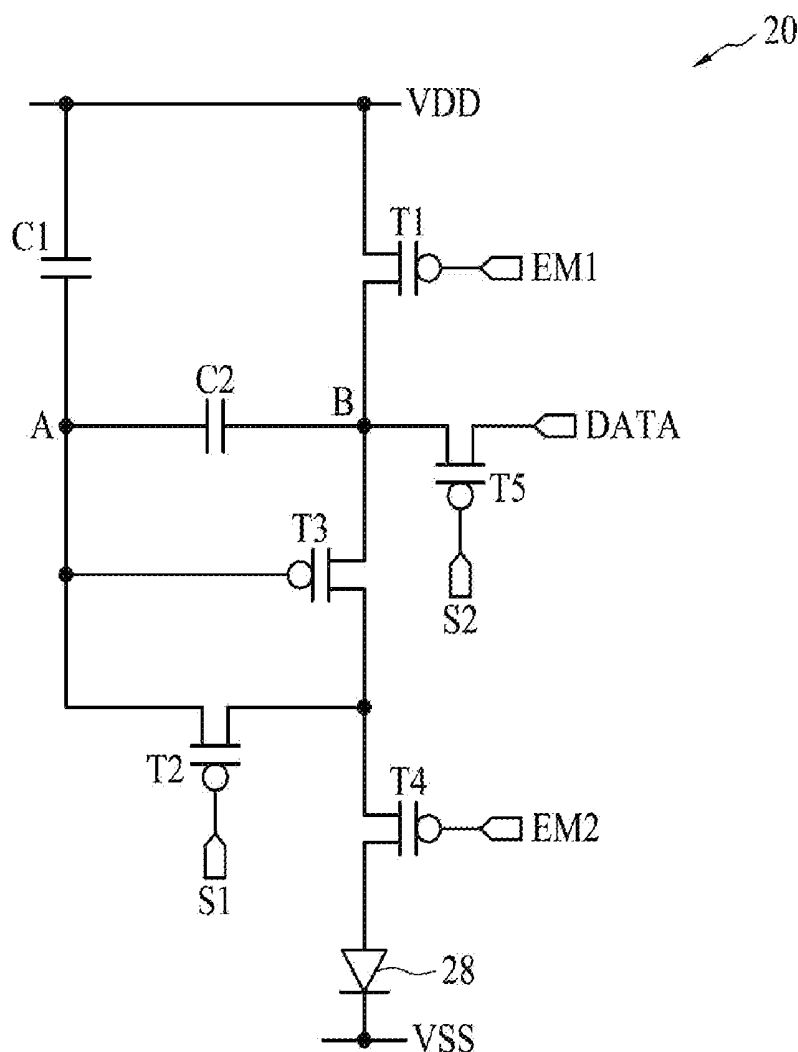


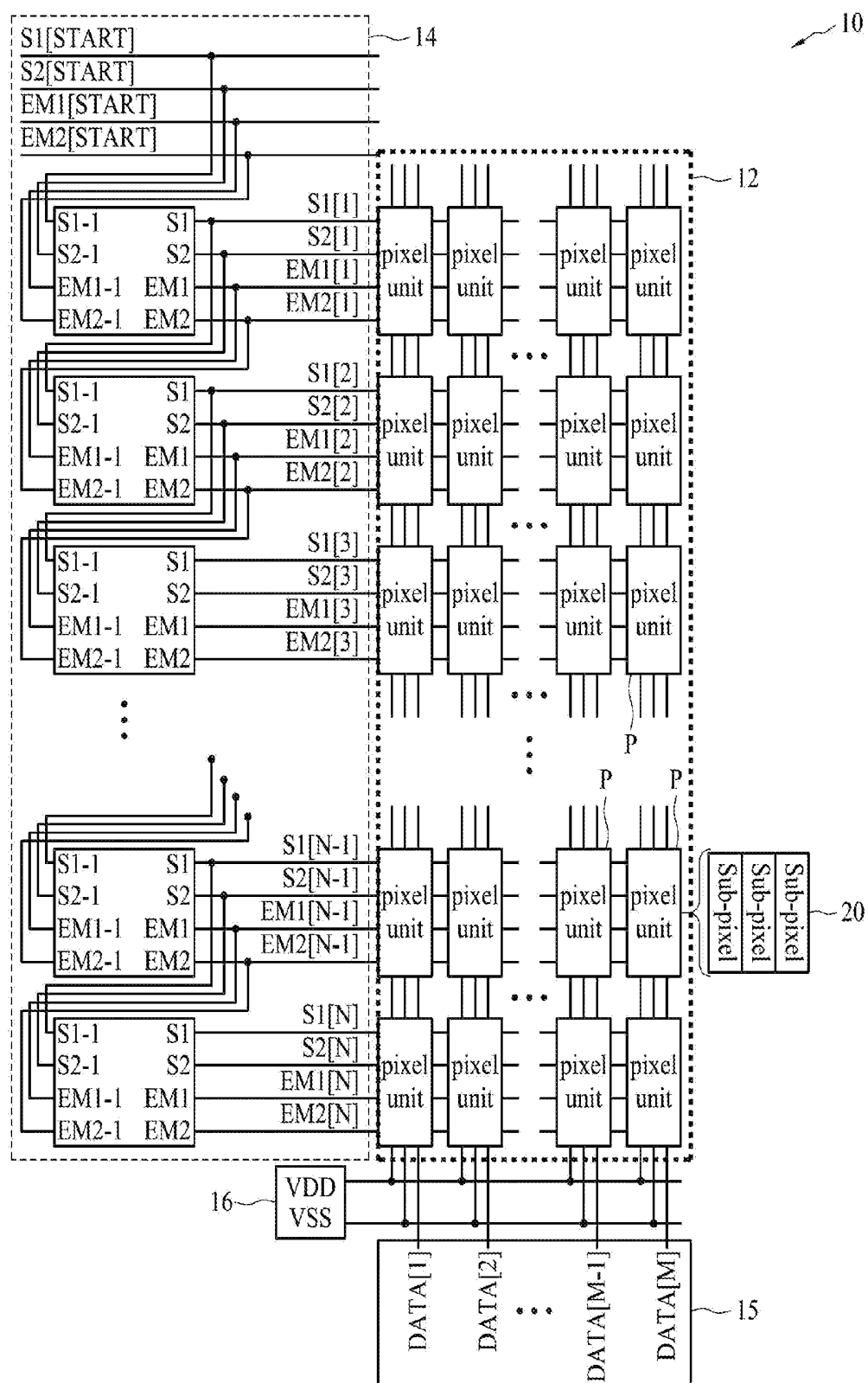


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CHENG(10) **Pub. No.: US 2018/0137816 A1**(43) **Pub. Date: May 17, 2018**(54) **PIXEL CIRCUIT IN AN
ELECTROLUMINESCENT DISPLAY**(52) **U.S. Cl.**
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14, 2016.**Publication Classification**(51) **Int. Cl.**
G09G 3/3233 (2006.01)
H01L 27/32 (2006.01)(57) **ABSTRACT**

A circuit includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor is coupled between a supply voltage and the first node. The second capacitor is coupled between the first node and the second node. The first capacitor and the second capacitor are configured to establish a compensation voltage associated with a threshold voltage of the transistor at the gate of the transistor in response to a first control signal, and establish the compensation voltage at the first terminal of the transistor in response to a second control signal. The transistor is configured to pass a current through the EL device. Moreover, the current has a magnitude independent of the threshold voltage of the transistor.





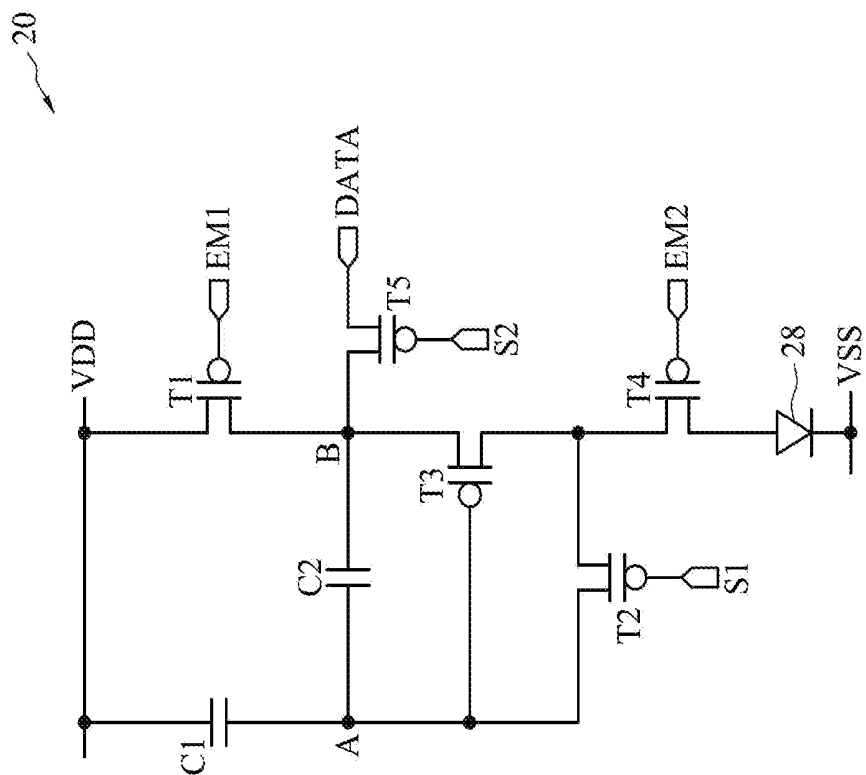


FIG. 2

20

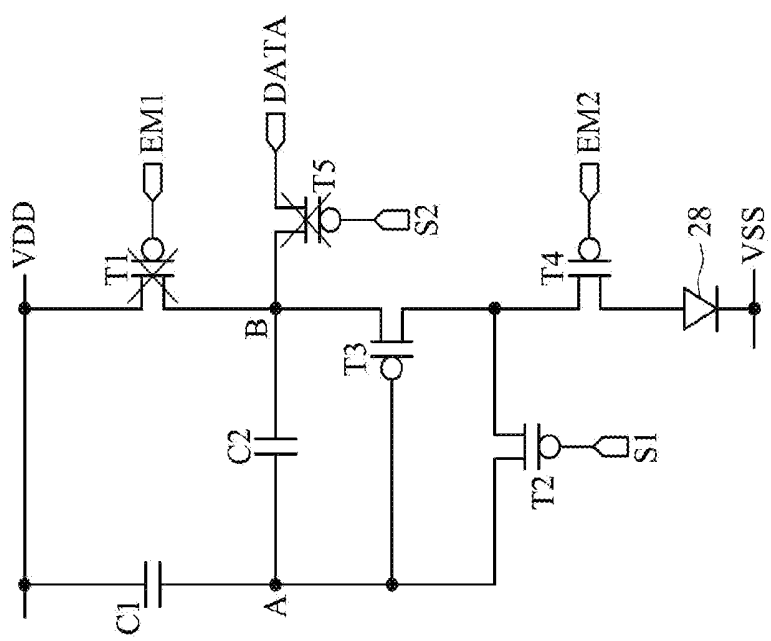


FIG. 3B

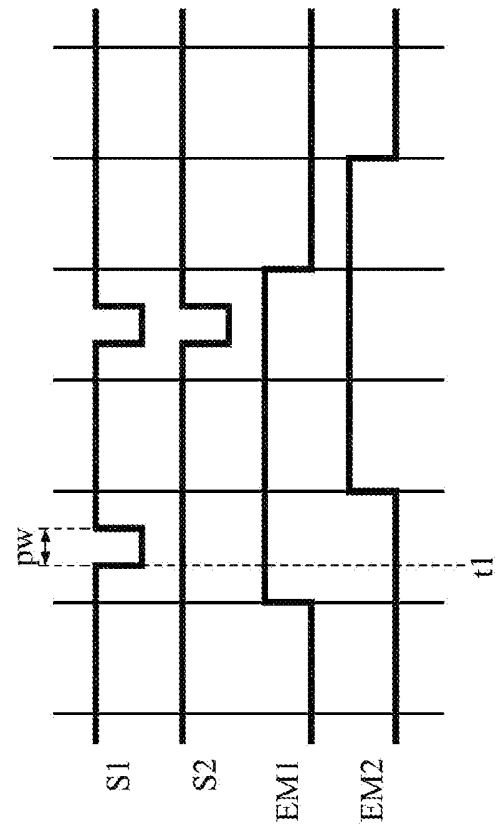


FIG. 3A

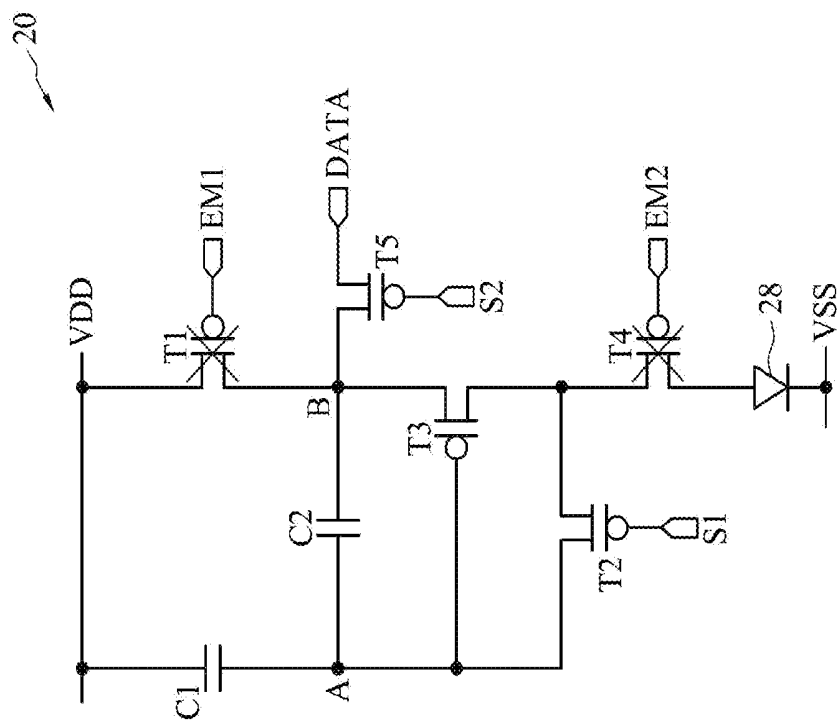


FIG. 4B

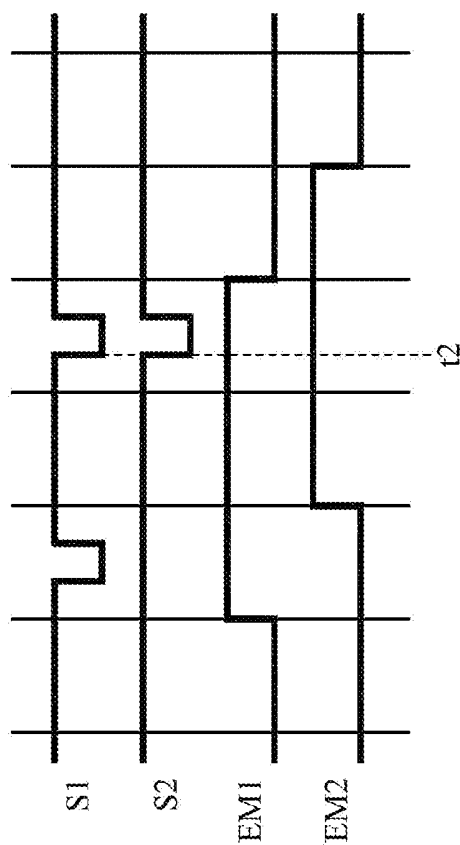


FIG. 4A

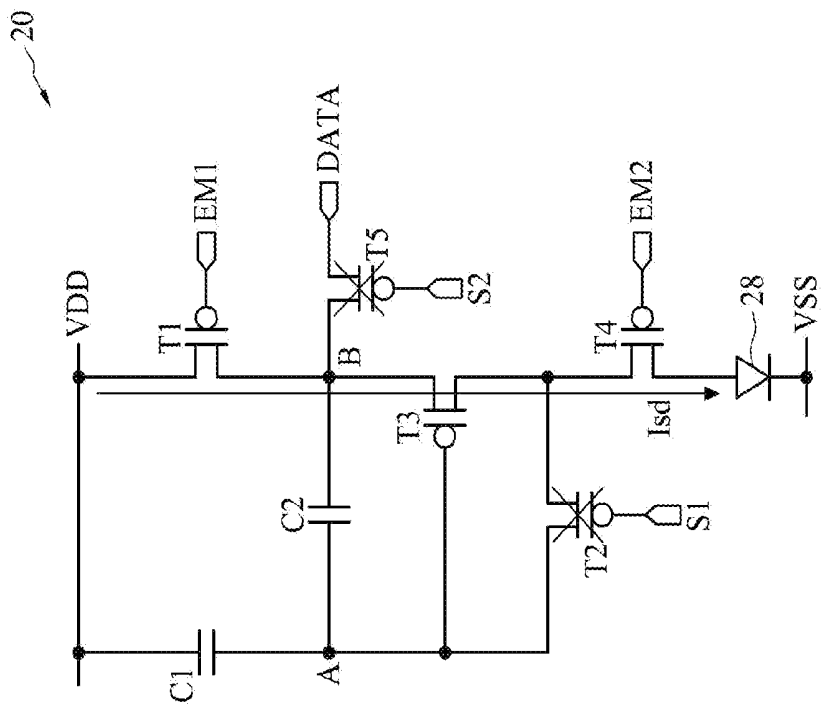


FIG. 5B

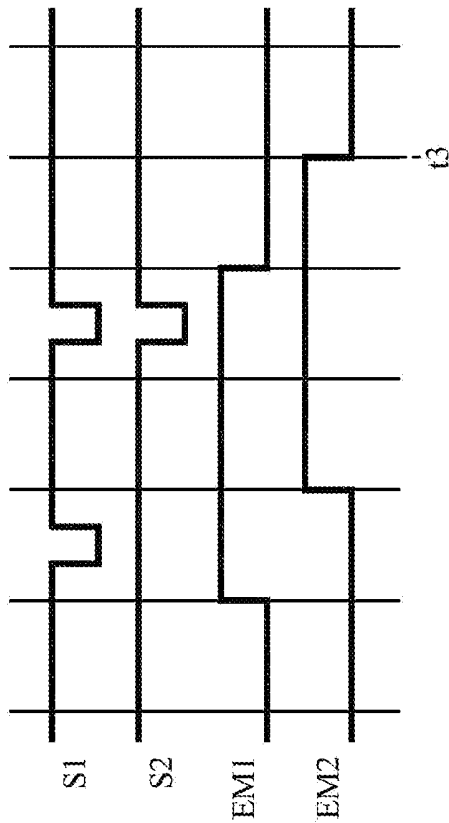


FIG. 5A

60

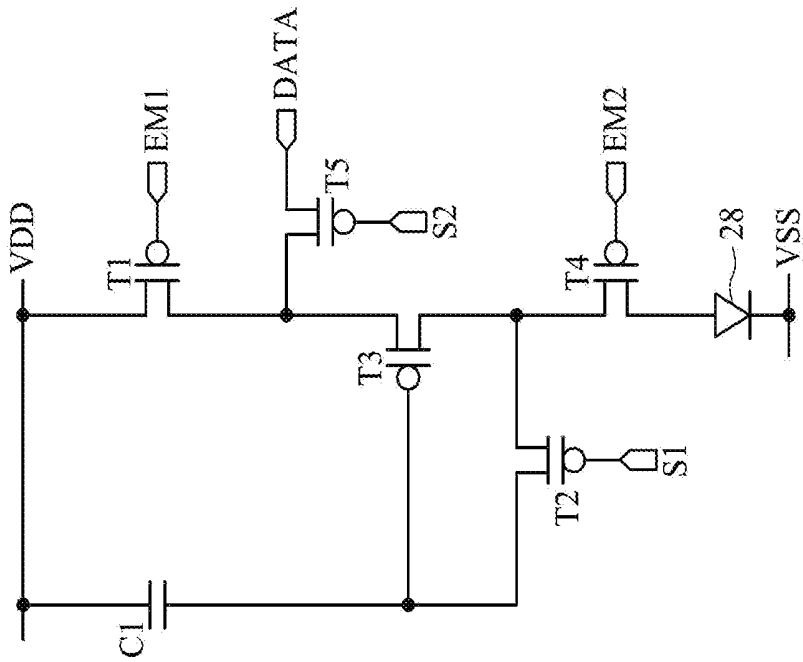


FIG. 6

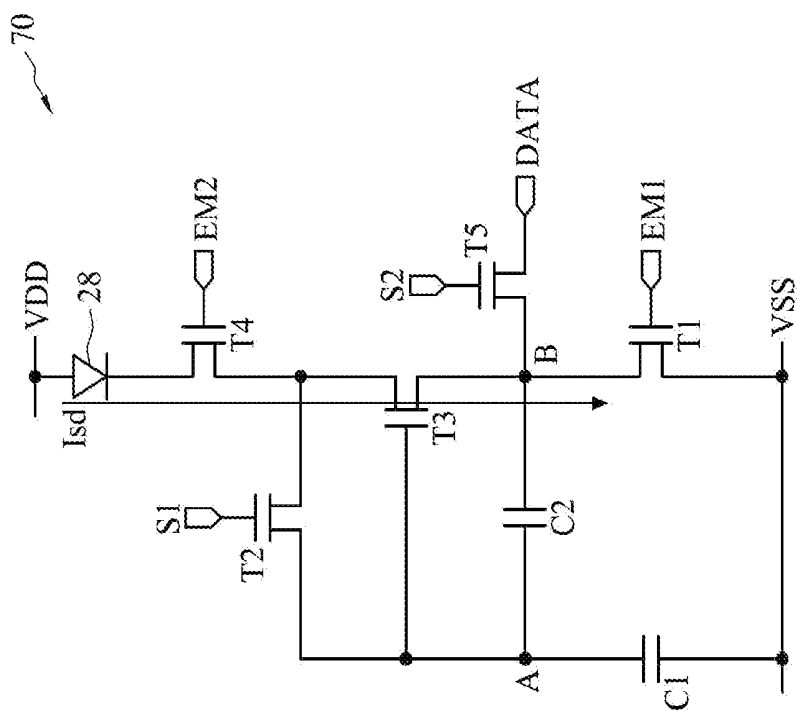


FIG. 7A

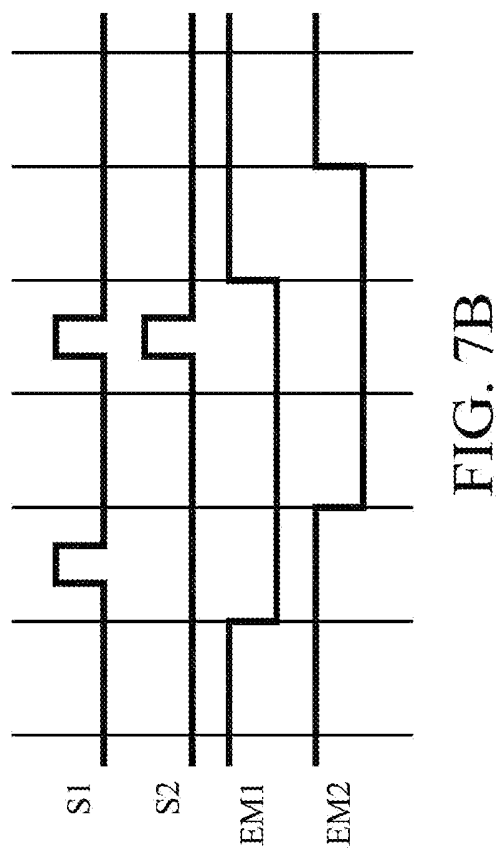


FIG. 7B

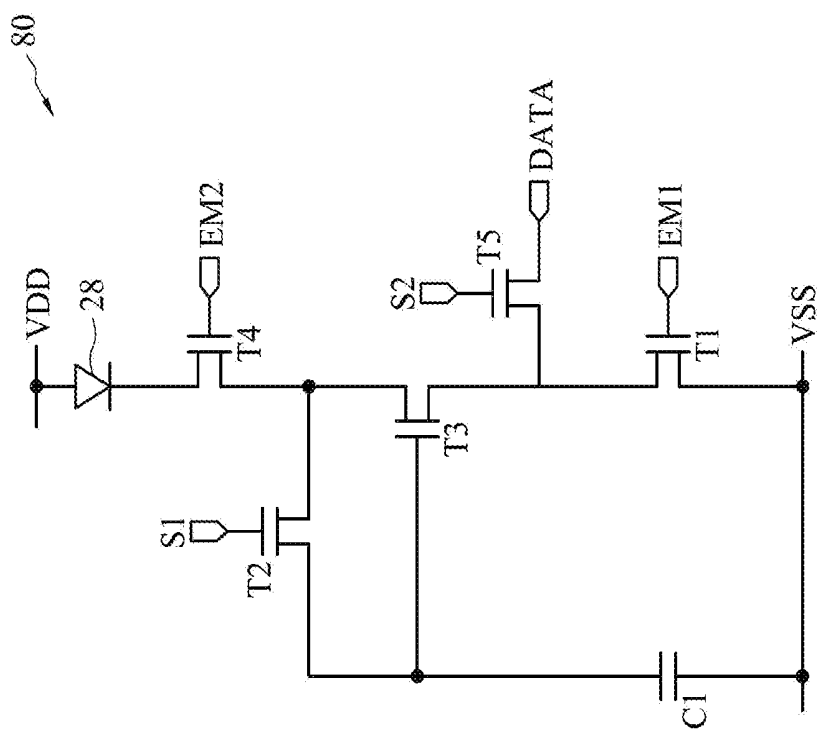


FIG. 8

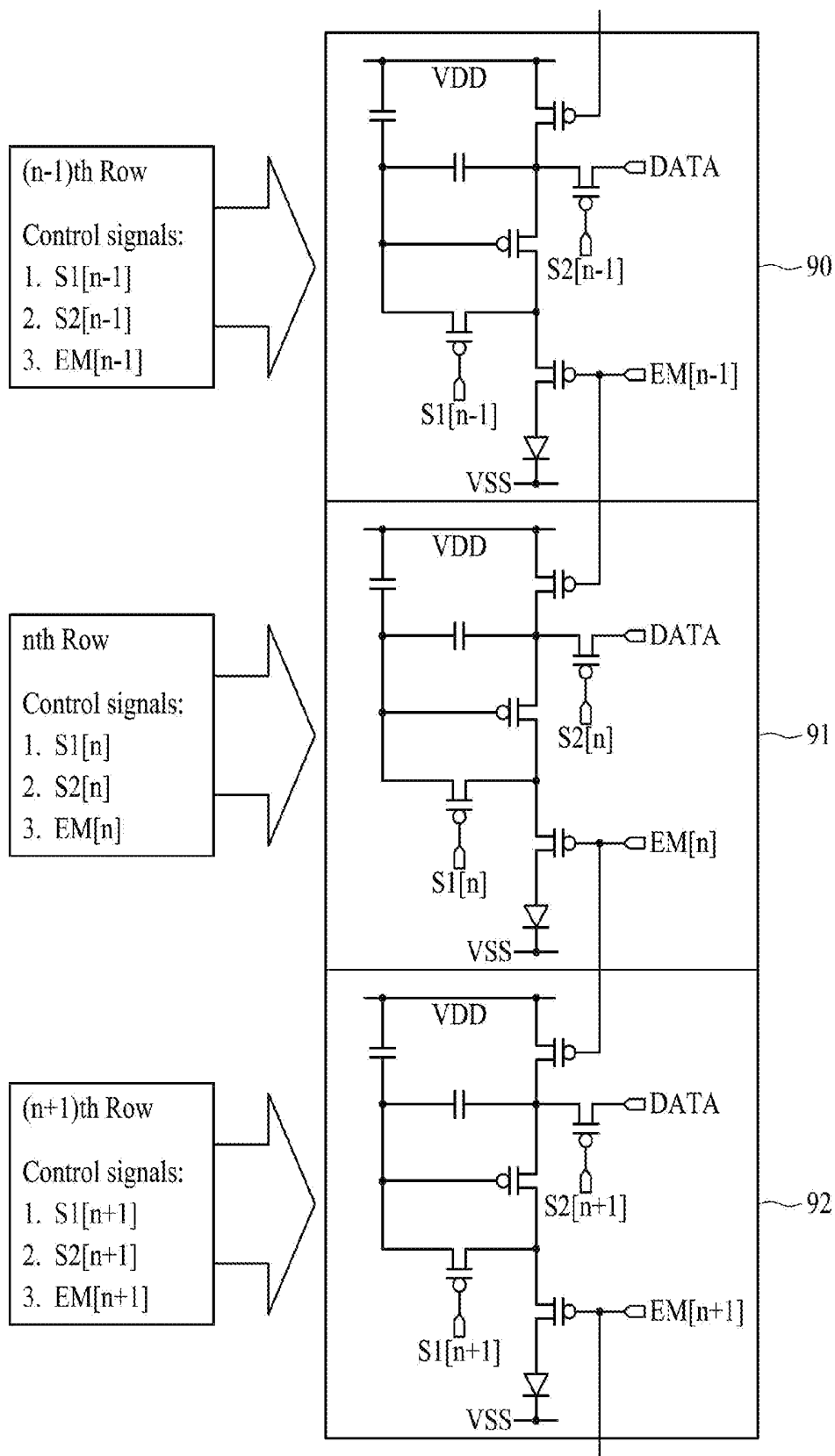


FIG. 9

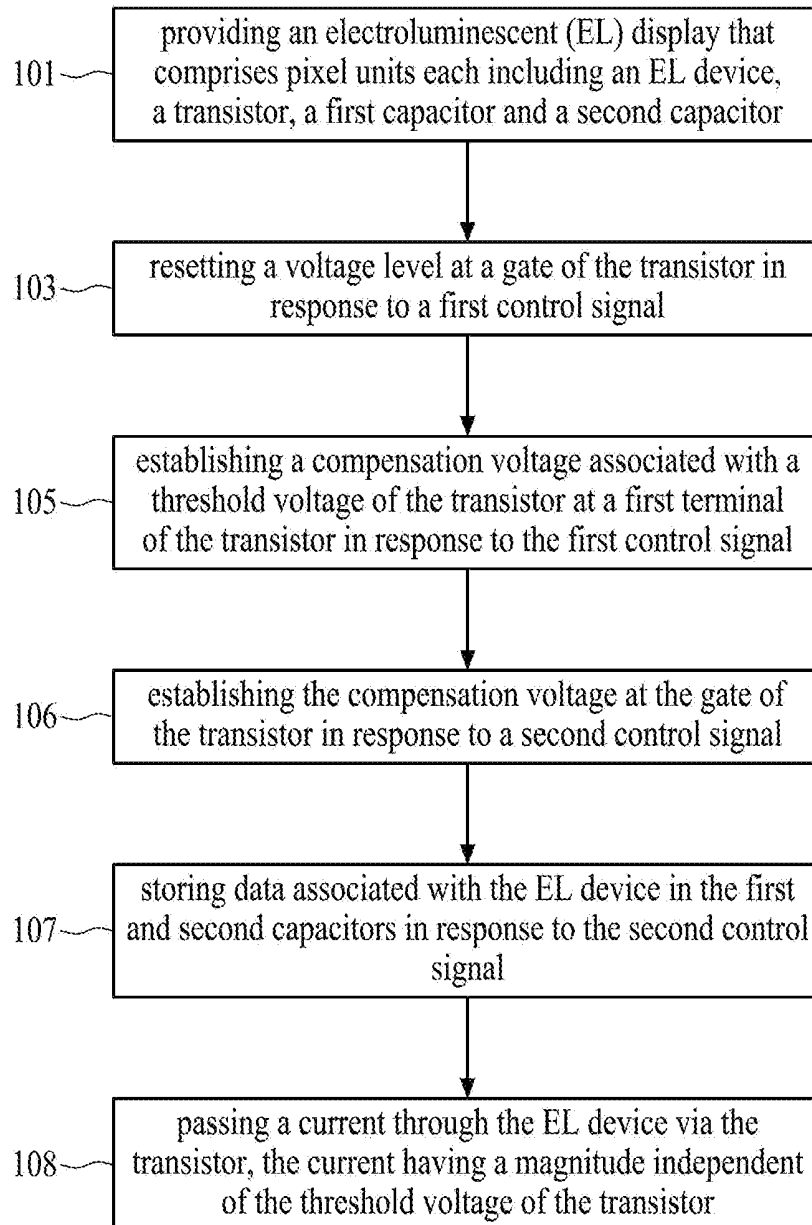


FIG. 10

PIXEL CIRCUIT IN AN ELECTROLUMINESCENT DISPLAY

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. provisional application Ser. No. 62/421,435, filed Nov. 14, 2016, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND

[0002] An electroluminescent (EL) display, such as an active matrix organic light emitting diode (AMOLED) display, may include an array of pixels. Each of the pixels may include an EL device, a switching transistor for transfer data that contains information on luminescence, and a driving transistor for driving the EL device to emit light according to the data. While such EL display enjoys the benefit of relatively low power consumption, display non-uniformity may exist among pixels due to process factors in semiconductor manufacturing. It may thus be desirable to have a circuit that solves the problem.

SUMMARY

[0003] Embodiments of the present invention provide a circuit that includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor is coupled between a supply voltage and the first node. The second capacitor is coupled between the first node and the second node. The first capacitor and the second capacitor are configured to establish a compensation voltage associated with a threshold voltage of the transistor at the gate of the transistor in response to a first control signal, and establish the compensation voltage at the first terminal of the transistor in response to a second control signal. The transistor is configured to pass a current through the EL device. Moreover, the current has a magnitude independent of the threshold voltage of the transistor.

[0004] In an embodiment, the circuit further includes a transistor configured to reset a voltage level at the gate of the transistor in response to the first control signal.

[0005] In another embodiment, the circuit further includes a transistor configured to receive data associated with the EL device in response to the second control signal.

[0006] In yet another embodiment, the circuit further includes a transistor configured to allow the current to pass through the EL device.

[0007] In still another embodiment, the magnitude of the current is a function of a capacitance each of the first and second capacitors.

[0008] In an embodiment, the transistor includes a p-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (VDD - V_{data}) \right]^2$$

[0009] where I_{sd} represents the magnitude of the current, k is constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VDD represents the

supply voltage, and V_{data} represents a voltage level of data associated with the EL device.

[0010] In another embodiment, the transistor includes an n-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (V_{data} - VSS) \right]^2$$

[0011] where I_{sd} represents the magnitude of the current, k is a constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and V_{data} represents a voltage level of data associated with the EL device.

[0012] In yet another embodiment, a pulse width of the first control signal is adjustable, and a pulse width of the second control signal is dependent of resolution of the display.

[0013] Some embodiments of the present invention provide an electroluminescent (EL) display that comprises an array of pixel units. Each of the pixel units includes an electroluminescent (EL) device, a transistor, a first capacitor and a second capacitor. The transistor includes a gate coupled to a first node and a first terminal coupled to a second node. The first capacitor is coupled between a supply voltage and the first node. The second capacitor is coupled between the first node and the second node. The first capacitor and the second capacitor are configured to establish a compensation voltage associated with a threshold voltage of the transistor at the gate of the transistor in response to a first control signal, and establish the compensation voltage at the first terminal of the transistor in response to a second control signal. The transistor is configured to pass a current through the EL device. Moreover, the current has a magnitude independent of the threshold voltage of the transistor.

[0014] In an embodiment, the EL display further includes a first transistor and a second transistor, which are configured to allow the current to pass through the EL device in response to a third control signal and a fourth control signal, respectively.

[0015] In another embodiment, the array of pixel units includes a first pixel unit on an $(N-1)$ -th row of the array and a second pixel unit on an N -th row of the array and immediately adjacent to the first pixel unit, N being a natural number. The fourth control signal provided to the first pixel unit serves as the third control signal for the second pixel unit.

[0016] Embodiments of the present invention also provide a method of voltage compensation in an electroluminescent (EL) display that comprises an array of pixel units each including an EL device, a transistor, a first capacitor and a second capacitor. The method includes establishing a compensation voltage associated with a threshold voltage of the transistor at a first terminal of the transistor in response to a first control signal, establishing the compensation voltage at a gate of the transistor in response to a second control signal, storing data associated with the EL device in the first and second capacitors in response to a third control signal, and passing a current through the EL device via a first transistor and a fourth transistor in response to a third control signal and a fourth control signal, respectively. The current has a magnitude independent of the threshold voltage the transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0018] FIG. 1 is a block diagram of a display, in accordance with an embodiment.

[0019] FIG. 2 is a circuit diagram of a sub-pixel unit in the display illustrated in FIG. 1, in accordance with an embodiment.

[0020] FIGS. 3A and 3B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a first phase, in accordance with some embodiments.

[0021] FIGS. 4A and 4B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a second phase, in accordance with some embodiments.

[0022] FIGS. 5A and 5B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a third phase, in accordance with some embodiments.

[0023] FIG. 6 is a circuit diagram of a sub-pixel unit in the display illustrated in FIG. 1, in accordance with another embodiment.

[0024] FIG. 7A is a circuit diagram of a sub-pixel unit in the display illustrated in FIG. 1, in accordance with still another embodiment.

[0025] FIG. 7B is a timing diagram of control signals for operating the circuit illustrated in FIG. 7A, in accordance with some embodiments.

[0026] FIG. 8 is a circuit diagram of a sub-pixel unit in the display illustrated in FIG. 1, in accordance with yet another embodiment.

[0027] FIG. 9 is a circuit diagram of a sub-pixel unit, in accordance with an embodiment.

[0028] FIG. 10 is a flow diagram showing a method of voltage compensation in an electroluminescent display.

DETAILED DESCRIPTION

[0029] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0030] Further, it will be understood that when an element is referred to as being “connected to” or “coupled to” another element, it may be directly connected to or coupled to the other element, or intervening elements may be present.

[0031] In the below description, a signal is asserted with a logical high value to activate a corresponding device when the device is active high. In contrast, the signal is deasserted with a low logical value to deactivate the corresponding device. When the device is active low, however, the signal is asserted with a low logical value to activate the device, and is deasserted with a high logical value to deactivate the device.

[0032] FIG. 1 is a block diagram of a display 10, in accordance with an embodiment. The display 10 may include an electroluminescent (EL) display, for example, an active matrix organic light emitting diode (AMOLED) display.

[0033] Referring to FIG. 1, the display 10 includes an active area 12, a gate driver 14 and a source driver 15. The active area 12 includes an array of pixel units P arranged in, for example, an N×M matrix. The gate driver 14 provides control signals S1, S2, EM1 and EM2 through N scan lines to the N rows of pixel units. The source driver 15 provides data to a selected pixel of the M columns of pixel units through data lines DATA[1] to DATA[M]. Moreover, a power driver 16 provides supply voltages in a power rail of VDD and VSS to the active area 12. In an embodiment, VDD is approximately five volts (5V), and VSS is approximately -5V.

[0034] Each of the pixel units P in the active area 12 includes three sub-pixel units 20, which may be used to display color red (R), color green (G) and color blue (B). In other embodiments, for example, in a sub-pixel rendering (SPR) sensor, the number of sub-pixel units is not limited to three. In the present embodiment, the three sub-pixels 20 are arranged along the row direction. Accordingly, the number of data lines for the source driver 15 is 3×M.

[0035] FIG. 2 is a circuit diagram of an exemplary sub-pixel unit 20 in the display 10 illustrated in FIG. 1, in accordance with an embodiment.

[0036] Referring to FIG. 2, the circuit includes an EL device 28, transistors T1 to T5, a first capacitor C1 and a second capacitor C2. The EL device 28 includes, for example, a current-driven element that may include an organic light emitting diode (OLED), a micro LED or a quantum dot LED (QLED). The first capacitor C1 and the second capacitor C2 serve as storage capacitors. The transistor T3 serves as a driving transistor to drive the EL device 28 according to data stored in the first and second capacitors C1 and C2. In the present embodiment, each of the transistors T1 to T5 includes a p-type thin film transistor (TFT) or a p-type metal-oxide-semiconductor (PMOS) transistor.

[0037] A gate of the transistor T2 receives a first control signal S1. A drain of the transistor T2 is coupled to a first node A. In addition, a gate of the transistor T3 is coupled to the first node A and hence the drain of the transistor T2. A source of the transistor T3 is coupled to a second node B. A drain of the transistor T3 is coupled to a source of the transistor T2. Persons having ordinary skill in the art will understand that drain and source terminals of a MOS transistor may be interchangeable, depending on voltage levels applied thereto.

[0038] Moreover, a gate of the transistor T5 receives a second control signal S2. A source of the transistor T5 receives data (labeled “DATA”) on a corresponding data line from the source driver 15 in response to the second control signal S2. A drain of the transistor T5 is coupled to the second node B and hence the source of the transistor T3. In

addition, a gate of the transistor T1 receives a third control signal EM1. A source of the transistor T1 receives a supply voltage VDD. A drain of the transistor T1 is coupled to the second node B and hence the drain of the transistor T5 and also the source of the transistor T3. Further, a gate of the transistor T4 receives a fourth control signal EM2. A source of the transistor T4 is coupled to the drain of the transistor T3 and hence the source of the transistor T2. A drain of the transistor T4 is coupled to an anode of the EL device 28. A cathode of the EL device 28 receives another supply voltage VSS.

[0039] The first capacitor C1 includes a first end to receive VDD and a second end coupled to the first node A. In addition, the second capacitor C2 includes a first end coupled to the first node A, and a second end coupled to the second node B.

[0040] FIGS. 3A and 3B are diagrams showing a method of operating the circuit 20 illustrated in FIG. 2 in a first phase, in accordance with some embodiments.

[0041] Referring to FIG. 3A, the control signals S1, S2, EM1 and EM2 are configured to be active low in view of the p-type transistors T1 to T5. At time t1, the first control signal S1 is asserted at a falling edge, the second and third control signals S2 and EM1 kept at a high logical level are not asserted, and the fourth control signal EM2 is kept at a low logical level. As a result, referring to FIG. 3B, the transistors T2 and T4 are turned on, while the transistors T1 and T5 are turned off (a cross sign "X" labeled). Since the transistors T2 and T4 are turned on, a voltage level at the first node A (denoted as VA), and hence a voltage level at the gate of the transistor T3 (denoted as Vg), is pulled to VSS+|Vth_EL|, where |Vth_EL| is the threshold voltage of the EL device 28. In addition, a voltage level at the second node B (denoted as VB), and hence a voltage level at the source of the transistor T3 (denoted as Vs), is VSS+|Vth_EL|+|Vth3|, where |Vth3| is the threshold of driving transistor T3. Moreover, in a previous phase (the third phase to be discussed in FIGS. 5A and 5B), the voltage level of Vg satisfies Vg>VSS+|Vth_EL| so as to keep the transistor T3 at an on state.

[0042] Accordingly, during the first phase, VA (Vg) is reset to VSS+|Vth_EL|. Moreover, a first compensation is made to pull VB (Vs) to VSS+|Vth_EL|+|Vth3|. The threshold voltage of the driving transistor T3, |Vth3|, which serves as a compensation voltage, is established at the second node B during the first phase. VB or Vs can reach a desirable value of VSS+|Vth_EL|+|Vth3| by means of adjusting a pulse width pw of the first control signal S1. The pulse width pw of the first control signal S1 is a time period that the first control signal S1 stays activated. The time for establishing the compensation voltage, hereinafter "the compensation time," is positively proportional to the pulse width pw of the first control signal S1. Since the display 10 provides a refresh rate of 60 hertz (Hz) or 16.7 milliseconds (ms), which is perceivable to human vision, the resolution of the display 10 is defined as 16.7 ms/N, N being the number of rows of pixel units P in the display 10. As the display 10 gets more advanced, the value of N becomes larger and hence the resolution becomes smaller, which results in a more rigid compensation time. In existing displays, a higher resolution may mean a shorter compensation time. With the pulse width pw of the first control signal S1 being adjustable, the compensation time is not limited by the resolution of the display 10. As the compensation time becomes longer, the voltage level of VB reaches closer to the saturation voltage of the second capacitor C2, which alleviates the problem of rigid compensation time and enhances the display quality of the display 10.

[0043] FIGS. 4A and 4B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a second phase, in accordance with some embodiments.

[0044] Referring to FIG. 4A, at time t2, the first and second control signals S1 and S2 are asserted, the third control signal EM1 stays at a high logical level, and the fourth control signal EM2 is not asserted. As a result, referring to FIG. 4B, the transistors T2 and T5 are turned on, and the transistors T1 and T4 are turned off. Since the transistor T5 is turned on, data is written to the second node B. Accordingly, VB (Vs) becomes Vdata, a voltage level of DATA to cause the EL device 28 to emit light accordingly. In addition, by the coupling function of the second capacitor C2, VA (Vg) becomes VDD-|Vth3|. With the second capacitor C2, a second compensation is effectively made on the basis of |Vsg| of the transistor T3, which substantially equals |Vth3|. By comparison, for a circuit absent from the second capacitor C2, no such basis of |Vsg| is established when a second compensation is made. Accordingly, the second capacitor C2 facilitates an efficient and faster compensation.

[0045] While the compensation time for the first compensation is not limited by the resolution of a display, the compensation time for the second compensation depends on the resolution and may be, for example, shorter than a line time that equals 16.7 ms/N. Moreover, as the first compensation time is positively proportional to the pulse width of the first control signal S1, the second compensation time is positively proportional to the pulse width of the second control signal S2.

[0046] FIGS. 5A and 5B are diagrams showing a method of operating the circuit illustrated in FIG. 2 in a third phase, in accordance with some embodiments.

[0047] Referring to FIG. 5A, at time t3, the fourth control signal EM2 is asserted and the third control signal EM1 is logically low, while the first and second control signals S1 and S2 are not asserted. As a result, referring to FIG. 5B, the transistors T1 and T4 are turned on, and the transistors T2 and T5 are off. Since the transistor T1 is turned on, VB (Vs) becomes VDD. As VB changes from Vdata (second phase) to VDD (third phase), by function of the first and second capacitors C1 and C2, VA (Vg) becomes

$$Vdata - |Vth3| + \left[\frac{C2}{C1 + C2} \times (VDD - Vdata) \right],$$

in which C1 and C2 also represent capacitances of the first and second capacitors C1 and C2, respectively.

[0048] Moreover, a current Isd flows from the supply power VDD through the EL device 28 to VSS via the transistors T1, T3 and T4. The current Isd can be expressed in equation (1) below.

$$|Isd| = k \times (|Vsg| - |Vth3|)^2 \quad \text{equation (1)}$$

[0049] where k is a constant. Since

$$Vsg = Vs - Vg = VB - VA = |Vth3| + \left[\frac{C1}{C1 + C2} \times (VDD - Vdata) \right],$$

equation (1) is rearranged in equation (2) as follows.

$$|Isd| = k \times \left[\frac{C1}{C1 + C2} \times (VDD - Vdata) \right]^2 \quad \text{equation (2)}$$

[0050] Since equation (2) is free of the V_{th} term, display quality of the display 10 is enhanced.

[0051] FIG. 6 is a circuit diagram of a sub-pixel unit 60 in the display 10 illustrated in FIG. 1, in accordance with another embodiment.

[0052] Referring to FIG. 6, the circuit is similar to that described and illustrated with reference to FIG. 2 except that, for example, the second capacitor C2 is absent, resulting in a five-transistor-one-capacitor (5T1C) circuit structure. The 5T1C circuit structure works normally as the 5T2C circuit structure illustrated in FIG. 2 except the function of fast compensation.

[0053] FIG. 7A is a circuit diagram of a sub-pixel unit 70 in the display 10 illustrated in FIG. 1, in accordance with still another embodiment.

[0054] Referring to FIG. 7A, the circuit is similar to the circuit described and illustrated with reference to FIG. 2 except that, for example, n-type TFTs or NMOS transistors replace the PMOS transistors T1 to T5 in FIG. 2. Specifically, a gate of the transistor T2 receives a first control signal S1. A source of the transistor T2 is coupled to a first node A. In addition, a gate of the transistor T3 is coupled to the first node A and hence the source of the transistor T2. A source of the transistor T3 is coupled to a second node B. A drain of the transistor T3 is coupled to a drain of the transistor T2.

[0055] Moreover, a gate of the transistor T5 receives a second control signal S2. A drain of the transistor T5 receives data (labeled "DATA") on a corresponding data line from the source driver 15 in response to the second control signal S2. A source of the transistor T5 is coupled to the second node B and hence the source of the transistor T3. In addition, a gate of the transistor T1 receives a third control signal EM1. A source of the transistor T1 receives a supply voltage VSS. A drain of the transistor T1 is coupled to the second node B and hence the source of the transistor T5 and also the source of the transistor T3. Further, a gate of the transistor T4 receives a fourth control signal EM2. A source of the transistor T4 is coupled to the drain of the transistor T3 and hence the drain of the transistor T2. A drain of the transistor T4 is coupled to a cathode of the EL device 28. An anode of the EL device 28 receives another supply voltage VDD.

[0056] The first capacitor C1 includes a first end to receive VSS and a second end coupled to the first node A. In addition, the second capacitor C2 includes a first end coupled to the first node A, and a second end coupled to the second node B.

[0057] FIG. 7B is a timing diagram for operating the circuit illustrated in FIG. 7A, in accordance with some embodiments.

[0058] Referring to FIG. 7B, the control signals S1, S2, EM1 and EM2 are similar to those described and illustrated with reference to FIG. 3A, 4A or 5A except that, for example, the control signals S1, S2, EM1 and EM2 in FIG. 7B are active high or asserted at a rising edge.

[0059] In operation, during the first phase, VA (Vg) is reset to $VDD - |V_{th_EL}|$, and VB (Vs) due to a first compensation reaches $VDD - |V_{th_EL}| - |V_{th3}|$. In addition, during the second phase, VB (Vs) is written to Vdata, and VA (Vg) due to a second compensation reaches $Vdata + |V_{th3}|$. Subsequently, during the third phase, VB (Vs) becomes VSS, while VA (Vg) is

$$Vdata - |V_{th3}| + \left[\frac{C2}{C1 + C2} \times (VSS - Vdata) \right].$$

[0060] A current I_{sd} flowing through the EL device in FIG. 7A can be expressed in equation (3) below.

$$|I_{sd}| = k \times (|V_{gs}| - |V_{th3}|)^2 = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS) \right]^2 \quad \text{equation (3)}$$

[0061] FIG. 8 is a circuit diagram of a sub-pixel unit 80 in the display 10 illustrated in FIG. 1, in accordance with yet another embodiment.

[0062] Referring to FIG. 8, the circuit is similar to that described and illustrated with reference to FIG. 7A except that, for example, the second capacitor C2 is absent. The 5T1C circuit structure works normally as the 5T2C circuit structure illustrated in FIG. 7A except the function of fast compensation.

[0063] FIG. 9 is a diagram of a circuit structure of sub-pixel units, in accordance with an embodiment.

[0064] Referring to FIG. 9, the circuit structure is similar to that described and illustrated with reference to FIG. 2 except that, for example, sub-pixel units arranged along the column direction are configured to receive a fourth control signal EM2, that is provided to an immediately adjacent sub-pixel unit on a previous row, as a third control signal EM1. For discussion, only exemplary sub-pixel units 90, 91 and 92 are shown. In the sub-pixel unit 91, for example, a third control signal EM[n] that would otherwise be provided to a sub-pixel unit on an n-th row as in FIG. 3A, 4A or 5A is replaced by a fourth control signal EM[n-1] provided to a sub-pixel unit on an (n-1)-th row. Specifically, for the sub-pixel unit 91, a fourth control signal EM[n+1] provided to the sub-pixel unit 90 also serves as a third control signal coupled to the gate of the transistor T1 in the sub-pixel unit 91. In addition, for the sub-pixel unit 92, a fourth control signal EM[n] provided to the sub-pixel unit 91 also serves as a third control signal coupled to the gate of the transistor T1 in the sub-pixel unit 92. Effectively, the control mechanism is simplified.

[0065] FIG. 10 is a flow diagram showing a method of voltage compensation in an electroluminescent display.

[0066] Referring to FIG. 10, in operation 101, an electroluminescent (EL) display is provided. The EL display includes an array of pixel units each including an EL device, a transistor, a first capacitor and a second capacitor.

[0067] Next, in operation 103, a voltage level at a gate of the transistor is reset in response to a first control signal. In an embodiment, the transistor includes a p-type transistor, and Vg is reset to $VSS + |V_{th_EL}|$. In another embodiment, the transistor includes an n-type transistor, and Vg is reset to $VDD - |V_{th_EL}|$.

[0068] In operation 105, a compensation voltage associated with a threshold voltage of the transistor is established at a first terminal of the transistor in response to the first control signal.

[0069] Then, in operation 106, the compensation voltage is established at the gate of the transistor in response to a second control signal.

[0070] In operation 107, data associated with the EL device is stored in the first and second capacitors in response to the second control signal.

[0071] Subsequently, in operation 108, a current is passed through the EL device via the transistor. The current has a magnitude independent of the threshold voltage the transistor.

[0072] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A circuit, comprising:
an electroluminescent (EL) device;
a transistor including a gate coupled to a first node and a first terminal coupled to a second node;
a first capacitor, coupled between a supply voltage and the first node; and
a second capacitor, coupled between the first node and the second node,
wherein the first capacitor and the second capacitor are configured to establish a compensation voltage associated with a threshold voltage of the transistor at the gate of the transistor in response to a first control signal, and establish the compensation voltage at the first terminal of the transistor in response to a second control signal, and
wherein the transistor is configured to pass a current through the EL device, the current having a magnitude being independent of the threshold voltage of the transistor.
2. The circuit according to claim 1 further comprising a transistor configured to reset a voltage level at the gate of the transistor in response to the first control signal.
3. The circuit according to claim 1 further comprising a transistor configured to receive data associated with the EL device in response to the second control signal.
4. The circuit according to claim 1 further comprising a transistor configured to allow the current to pass through the EL device.
5. The circuit according to claim 1, wherein the magnitude of the current is a function of a capacitance each of the first and second capacitors.
6. The circuit according to claim 1, wherein the transistor includes a p-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (VDD - Vdata) \right]^2$$

where I_{sd} represents the magnitude of the current, k is a constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VDD represents the supply voltage, and $Vdata$ represents a voltage level of data associated with the EL device.

7. The circuit according to claim 1, wherein the transistor includes an n-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS) \right]^2$$

where I_{sd} represents the magnitude of the current, k is a constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and $Vdata$ represents a voltage level of data associated with the EL device.

8. The circuit according to claim 1, wherein a pulse width of the first control signal is adjustable, and a pulse width of the second control signal is dependent of resolution of the display.

9. An electroluminescent (EL) display, comprising:

an array of pixel units, each of the pixel units comprising:
an EL device;
a transistor including a gate coupled to a first node and a first terminal coupled to a second node;
a first capacitor, coupled between a supply voltage and the first node; and
a second capacitor, coupled between the first node and the second node,

wherein the first capacitor and the second capacitor are configured to establish a compensation voltage associated with a threshold voltage of the transistor at the gate of the transistor in response to a first control signal, and establish the compensation voltage at the first terminal of the transistor in response to a second control signal, and

wherein the transistor is configured to pass a current through the EL device, the current having a magnitude being independent of the threshold voltage of the transistor.

10. The electroluminescent display according to claim 9 further comprising a transistor configured to reset a voltage level at the gate of the transistor in response to the first control signal.

11. The electroluminescent display according to claim 9 further comprising a transistor configured to receive data associated with the EL device in response to the second control signal.

12. The electroluminescent display according to claim 9 further comprising a first transistor and a second transistor configured to allow the current to pass through the EL device in response to a third control signal and a fourth control signal, respectively.

13. The electroluminescent display according to claim 12, wherein the array of pixel units includes a first pixel unit on an $(N-1)$ -th row of the array and a second pixel unit on an N -th row of the array and immediately adjacent to the first pixel unit, N being a natural number, and wherein the fourth control signal provided to the first pixel unit serves as the third control signal for the second pixel unit.

14. The electroluminescent display according to claim 9, wherein the magnitude of the current is a function of a capacitance each of the first and second capacitors.

15. The electroluminescent display according to claim 9, wherein the transistor includes a p-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (VDD - Vdata) \right]^2$$

where I_{sd} represents the magnitude of the current, k is a constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VDD represents the supply voltage, and $Vdata$ represents a voltage level of data associated with the EL device.

16. The electroluminescent display according to claim **9**, wherein the transistor includes an n-type transistor, and the current is expressed as:

$$|I_{sd}| = k \times \left[\frac{C1}{C1 + C2} \times (Vdata - VSS) \right]^2$$

where I_{sd} represents the magnitude of the current, k is a constant, $C1$ and $C2$ represent capacitances of the first and second transistors, respectively, VSS represents the supply voltage, and $Vdata$ represents a voltage level of data associated with the EL device.

17. The electroluminescent display according to claim **9**, wherein a pulse width of the first control signal is adjustable, and a pulse width of the second control signal is dependent of resolution of the EL display.

18. A method of voltage compensation in an electroluminescent (EL) display that comprises an array of pixel units

each including an EL device, a transistor, a first capacitor and a second capacitor, the method comprising:

establishing a compensation voltage associated with a threshold voltage of the transistor at a first terminal of the transistor in response to a first control signal; establishing the compensation voltage at a gate of the transistor in response to a second control signal; storing data associated with the EL device in the first and second capacitors in response to a third control signal; and

passing a current through the EL device via a first transistor and a fourth transistor in response to a third control signal and a fourth control signal, respectively, the current having a magnitude independent of the threshold voltage the transistor.

19. The method according to claim **18**, wherein the array of pixel units includes a first pixel unit on an (N-1)-th row of the array and a second pixel unit on an N-th row of the array and immediately adjacent to the first pixel unit, N being a natural number, further comprising:

using the fourth control signal provided to the first pixel unit as the third control signal for the second pixel unit.

20. The method according to claim **19**, further comprising:

providing the first control signal having a pulse width that is adjustable; and

providing the second control signal having a pulse width that is dependent of resolution of the EL display.

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